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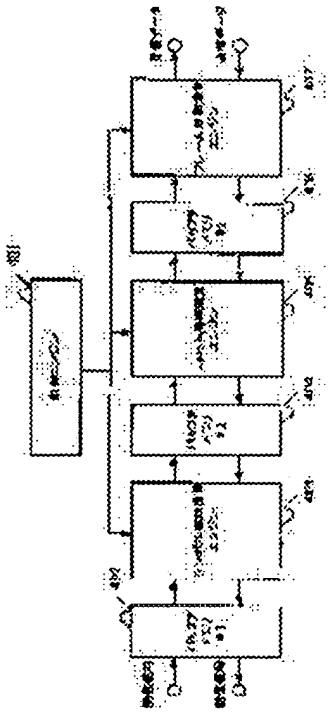
(54) COMMUNICATION EQUIPMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the scale of hardware by dividing modulation and demodulation processing in a base band part for every processing unit and processing plural channels in divided arithmetic units in time-multiplexing manner.

SOLUTION: Symbol period arithmetic engines 403 are plurally provided in parallel or a slot period arithmetic engine 405 is operated faster than a frame period arithmetic engine 407. A block required for modulation/demodulation processing is divided into each processing unit to allow the processing blocks to operate independent from each other. In addition, the received signals of the base band are stored in a first buffer memory 402 by the portion of several times of one symbol being the processing unit of the engine 403. Each engine is controlled by a control engine 401 and the respective engines 403, 405 and 407 asynchronously execute modulation/demodulation processing by the engine 401 and a channel to be processed is independent for every engine. Thus, the plural channels is highly efficiently modulated/demodulated in time-multiplexing manner.



* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the hardware and the software configuration of the communication device (a base station, terminal) which processes the data which communicate by two or more channels. It is suitable for the communication device especially used with the mobile communication system of a code division multiple access (CDMA:Code Division Multiple Access) method.
[0002]
[Description of the Prior Art] The configuration of the conventional base station used with CDMA mobile communication system is shown in drawing 12.
[0003] The input signal of the carrier frequency band received from the antenna 100 is changed into the input signal of baseband in the wireless section 101, and is inputted into the baseband section 134. Moreover, in the output composition section 107, it is superimposed on the sending signal of the baseband of each channel outputted from the baseband section 134, it is changed into the sending signal of a carrier frequency band in the wireless section 101, and is transmitted from an antenna 100.
[0004] The strange recovery processing section 102-1 which performs transceiver processing of one channel - s are prepared for the baseband section 134 by the number of channels (s) used in a base station. A matched filter (MF) 135 and one peak detecting element 136 are formed about two or more channels, and perform a pass search intermittently about each channel. The peak detecting element 136 chooses a large thing among the peaks (the receiving timing of a multi-pass is shown) of the correlation value outputted from MF. The selected pass timing is set as the correlation operation part 108-1 of the strange recovery processing section 102-1 of the channel which corresponds, respectively - s - n (n is the number of fingers), and the back-diffusion-of-gas processing for every finger is made.
[0005] Thus, circuit magnitude is made small by preparing MF in one multiple channel by performing a pass search about each channel periodically by time sharing in a base station. However, with this configuration, it has the strange recovery processing section 102 for every channel.
[0006] Moreover, there is a multi-code transmission mode which realizes high-speed transmission as a whole by multiplexing transmit data, using two or more low-speed transmission channels as the communicate mode in migration communication system. That baseband section will have the strange recovery processing section corresponding to two or more channels as well as [when a mobile station supports this multi-code transmission mode] the base station shown in drawing 12 .
[0007]
[Problem(s) to be Solved by the Invention] Thus, the baseband section 134 in the conventional communication device has the strange recovery processing section 102-1 according to the number of channels - s, and each strange recovery processing section was processing to juxtaposition. Therefore, in the case of a base station, in the case of the number of channels and mobile station to hold, there was a problem that hardware magnitude increased in proportion to the transmission speed at the time of multi-code transfer.

[0008] On the other hand, although the data-processing rate of LSI in recent years amounts also to 256MHz, although the data rate transmitted and received through a radio channel changes also with communication modes, it is only about 4MHz. Therefore, even if the operation speed of the baseband section 134 improves, constraint is received in a data rate after all, and the baseband section does not fully demonstrate data-processing capacity.
[0009] Furthermore, the block (correlation operation part 108 grade) which performs an operation per symbol, the block (detection section 111 grade) which performs an operation per slot, and the block (deinterleaver 115, error correction decoder 116 grade) which performs an operation per frame exist in the block which constitutes the strange recovery processing section 102-1 - s. However, in the strange recovery processing section 102, these blocks are connected serially and data processing from which a batch differs is serially performed by time series. Therefore, the large block of a batch had to wait for completion of data processing of a small block of a batch, and the dead time to which data processing is not carried out in the large block of a batch had produced it.
[0010]
[Means for Solving the Problem] carrying out reading appearance of the data from a storage means at a rate higher than the rate as which data are inputted into a storage means, and performing strange recovery processing at a high speed with a signal processor equipped with the storage means for memorizing the input signal of a multiple channel, and an operation means required for a strange recovery, in order to solve the above-mentioned problem -- processing of a multiple channel -- the time -- multiplex -- carrying out . processing of a multiple channel -- the time -- multiplex -- by being carried out, hardware magnitude is substantially reducible.
[0011]
[Embodiment of the Invention] A communication link format of the going-up circuit transmitted to drawing 11 from a mobile station in a W-CDMA system in a base station is shown. One 1105 (=10msec) is the base unit of channel codec processing of an interleave, error-correcting-code-izing, etc. One frame is divided into 16 slots. One slot 1106 (=0.625msec) is the base unit of air interface control, such as propagation way presumption and transmitted power control. One slot is divided into an inphase (I) component and a rectangular (Q) component, a data symbol 1101 is transmitted to I component, and the control symbol of pilot symbol 1102 grade is transmitted to Q component. One symbol 1107 is the base unit of the transmit data after channel codec processing. In a CDMA system, the diffusion sign (pseudo-random sign) called PN sequence to this symbol is multiplied, and a spread spectrum is performed. One chip 1108 is the base unit of a pseudo-random sign, and is the minimum unit in all processors.
[0012] (Example 1) The 1st operation gestalt of this invention is shown in drawing 1 . The case where it has three antenna 200-1-3 is illustrated. In the base station or mobile station which performs space diversity, and a multisector base station, it has two or more antennas. Space diversity compensates degradation of the input signal by phasing by receiving simultaneously the signal by which it comes from the same mobile station (or base station) with two or more antennas. the increase of the number of channels which can be held in a base station on the other hand when multisector-ization uses a diffusion sign which is different between a break and a sector in the service area (cel) of a base station into two or more sectors which have an each transceiver antenna -- carrying out -- frequency utilization effectiveness -- raising -- suppose like. Since two or more input signals are inputted to the baseband section 202 in any case, the channel (mobile station) which is going to perform a strange recovery needs to change an input by the selector 235 at every processing by of which diversity antenna a strange recovery is performed for whether it belongs to the service area which is which sector. In drawing 1 , the configuration of the base station at the time of multisector-izing is indicated.
[0013] each -- the input signal of the carrier frequency band received by antenna 200-1-3 is changed into the input signal of baseband by the wireless section 201. The input signal of baseband is stored in buffer memory 203-1-3 prepared for every antenna. Such buffer memory may be constituted as two or more memory, and may be constituted as two or more fields of one memory.
[0014] each -- storing of several times as much data as the maximum unit (for example, setting to a W-

CDMA system one frame) of recovery processing is enabled strangely buffer memory 203-1-3. The capacity of buffer memory is suitably defined with the number of channels which the gap of the data rate of a radio channel and the operation speed of the baseband section 202 and the dual modulation processing section 230 multiprocess. Moreover, the number of channels which can multiprocess the one baseband section is the following (data rate of the operation speed/radio channel of the baseband section).

[0015] Multiplex [of the data of all the channels of the total displacement station which is in the service area of an applicable sector] is carried out to the input signal of the baseband stored in buffer memory 203-1-3. This is repeated in the strange recovery processing section 230, and it is possible to perform recovery processing in which hardware magnitude was cut down and the data-processing rate of LSI was efficiently employed by reading and carrying out recovery processing. Moreover, the strange recovery processing section 230 modulates repeat transmit data, and the sending signal of the generated baseband is stored in buffer memory 203-1-3 for every sector. If the sending signal of the baseband of all the channels by which multiplex is carried out for every sector within LSI is stored in buffer memory 203-1-3, the sending signal of such baseband will be compounded about the sending signal of all LSI of a base station with the output composition vessel 207. The sending signal of the baseband by which multiplex was carried out is changed into the sending signal of a carrier frequency band in the wireless section 201, and is transmitted from an antenna 200. Thus, it is possible to perform modulation processing in which hardware magnitude was cut down and the data-processing rate of LSI was employed efficiently.

[0016] Hereafter, actuation of the baseband section 202 of drawing 1 is explained.

[0017] A control section (not shown) controls the baseband section 202 whole. As a content of control, assignment of the channel made into a strange recovery processing object, a transceiver sector, and an antenna etc. is included.

[0018] (1) Since over sampling technique of the recovery processing usual input signal is carried out, a signal is inputted by several times of a chip rate, and it is stored in buffer memory 203-1-3. If an input signal is written in to the predetermined capacity of buffer memory, return overwrite of it will be carried out to the first address. In a W-CDMA method (4MHz in chip rate), when it samples 4 times, the data rate inputted into buffer memory 203-1-3 is 16MHz. As for recovery processing of the input signal stored in buffer memory 203-1-3, processing is performed at the data-processing rate (for example, 256MHz) of the baseband section 202.

[0019] A selector 235 specifies the buffer memory 203 corresponding to the receiving antenna 200 which is the sector to which the channel to which it is going to restore belongs, and inputs an input signal into MF236 and the strange recovery processing section 230.

[0020] A pass search is made by MF236 and the peak detecting element 237, and the receiving timing which carries out back-diffusion of gas is given to the correlation operation part 208-1 - n. The correlation operation part 208-1 - n carry out the multiplication of an input signal (spread-spectrum signal) and the diffusion sign of a channel per chip to the given receiving timing, and accumulate the result per symbol (correlation operation). The detection section 211-1 - n detect the phase revolution produced in the propagation path with the pilot signal included in an input signal, arrange the phase of the multi-pass input signal (correlation operation part 208 output) by which back-diffusion of gas was carried out, and input it into the Rake composition section 214. Phase revolution detection processing in this detection section 211 is performed per slot. The Rake composition section 214 compounds the multi-pass input signal to which the phase was equal. In the case of the base station which performs space diversity, not only Rake composition of a multi-pass input signal but diversity composition which compounds the input signal of two or more antennas is performed in the Rake composition section 214.
 [0021] Sequential delivery is carried out and recovery processing of the input signal by which Rake composition was carried out is carried out at DEINTARIBA 215, the error correction decoder 216, and the error detection decoder 217. These decode coding processing and the signal which the interleave was carried out and was transmitted. Coding processing and an interleave are accomplished to the data of an one-frame unit, and decode processing is also performed considering one frame as a unit. The

signal with which error detection processing was made is outputted as received data.
[0022] (2) modulation **** -- the transmit data for one frame is first inputted into the error detecting code-ized machine 218. The error detecting code-ized machine 218 generates a CRC sign (Cyclic Redundancy Check) to this transmit data for one frame. The transmit data with which error detecting code was added is inputted into the error correcting code-ized machine 219. The error correcting code-ized machine 219 generates error correcting codes, such as a convolutional code and a Turbo sign, to the inputted data. The transmit data with which the error correcting code was added is inputted into an interleaver 220. An interleave is for mitigating the effect of the burst error produced in a propagation path by replacing and transmitting the sequence of transmit data.
[0023] The transmit format creation section 221 gives a pilot symbol and a transmitted power signal per slot to the interleaved sending signal according to a predetermined format (refer to drawing 11). The diffusion operation part 222 carries out the multiplication of a sending signal and the diffusion sign, and performs diffusion modulation processing. In the transmitted power control section 223, transmitted power control is performed based on the received transmitted power control information. Since the total power which can be transmitted with an antenna 200 is fixed, specifically, it assigns the rate of occupying to the total power of the power of the sending signal of each channel. Finally, the sending signal of each channel is stored in buffer memory 203-1-3.
[0024] (Example 2) The gestalt of operation of the 2nd of this invention is shown in drawing 2 . Only the baseband section is shown in drawing 2 . In the 1st operation gestalt, it has the description by CPU302 in the gestalt of this 2nd operation to wired logic having realized processing after a correlation operation at the point performed with software. In addition, it has two or more buffer memory 301, they are switched, and it outputs [in the case of one antenna, it is simplified, but / in processing two or more antennas] and inputs **/input signal between CPUs302. The processing performed to the signal of baseband mainly consists of multiplication and addition processing. Therefore, by software-izing these processings and processing in common by hardware called CPU302, it is possible to reduce hardware magnitude.
[0025] The flow chart of recovery processing is shown in drawing 3 . First, at the time of communication link initiation, peak detection of the pass search is performed and carried out for every channel, and the receiving timing of each finger is determined. Next, initializing of a channel is performed (step 1201). Setting out of a diffusion sign and a diffusion ratio, setting out of the receiving timing by pass search, etc. are included in initializing. The symbol unit processing 1202 is equivalent to processing by the correlation operation part 208 of drawing 1 . The slot unit processings 1203-1206 are equivalent to processing in the detection section 211 of drawing 1 , and the Rake composition section 214. The frame unit processings 1208-1210 are equivalent to processing with the frame unit processing blocks 215-217 of drawing 1 . After carrying out through these processings, a channel is changed, the above-mentioned processing is repeated and a multiple channel is processed.
[0026] The flow chart of modulation processing is shown in drawing 4 . By the transmitting system, by one frame, the loop of the frame unit processings 1301-1304 is carried out per all channels, and they are processed. Frame unit processing is equivalent to processing with the frame unit processing blocks 218-220 of drawing 1 of drawing 1 . Then, slot unit processing 1305 is performed by all channels. The slot unit processing 1305 is equivalent to processing with the transmit format creation vessel 221 of drawing 1 . Then, diffusion operation and transmitting output composition are performed by the symbol unit processings 1306 and 1307. This processing is equivalent to processing by the diffusion operation part 222 and the transmitted power control section 233 of drawing 1 . About a part for one symbol, the output of all channels is compounded and it transmits (step 1308). If the data of all the channels for one frame are processed to the last and broken, it will return to the beginning of a flow again.
[0027] (Example 3) The 3rd operation gestalt of this invention is shown in drawing 5 . Drawing 5 also shows only the baseband section and the case of one antenna is shown for simplification. Its attention is paid to the 3rd operation gestalt that processing of a symbol unit, processing of a slot unit, and processing of a frame unit have appeared one by one in strange recovery processing. It explains referring to drawing 1 .

[0028] As for the correlation operation part 208, the received data with which the input signal was inputted and back-diffusion of gas was carried out per symbol per chip are outputted. On the other hand, the detection section 211 and the Rake composition section 214 process to the received data for one slot (output of the correlation operation part 208). Furthermore, DEINTARIBA 215, the error correction decoder 216, and the error detection decoder 217 process to the received data for one frame (output of the Rake composition section 214).
[0029] Similarly, the error detecting code machine 218, the error correcting code machine 219, and INTARIBA 220 are processings of an one-frame unit, the transmit format creation machine 221 is processing of 1 slot unit, and the diffusion operation part 222 and the transmitted power control section 233 are processings in 1 symbol unit.
[0030] A block required for strange recovery processing is divided according to a batch, and a mutual processing block consists of this examples so that it can operate independently. When processing from which a batch differs like drawing 1 is serially given to a target, the processing speed of a symbol unit determines the whole processing speed, and, on the other hand, the utilization ratio of the hardware of big batches, such as a slot and a frame, has it. [low] Therefore, in this example, processing of the same batch is summarized to one block. And the hardware utilization ratio as the whole is raised by setting up suitably the working speed for every block, or the number of juxtaposition of a block. For example, two or more symbol period operation engines 403 are arranged in parallel, and are prepared. Or the slot period operation engine 405 is operated more quickly than the frame period operation engine 407.
[0031] The input signal of baseband is stored in the 1st buffer memory 402 a minute several times of one symbol which is the batch of the symbol period operation engine 403. In order to make change-over timing of processing regularity, even if it is the case where the die length of one symbol changes with channels, the input signal of a constant rate is inputted into the baseband section 202. For example, when it considers as the unit of processing of the die length for one symbol of a channel with the biggest symbol period, it processes by switching a channel to every at least 1 symbols (symbol period max) and a maximum of 16 symbols (in the case [Symbol period min and all] of W-CDMA).
[0032] The symbol period operation engine 403 is a block which performs strange recovery processing in a symbol unit. The symbol period operation engine 403 performs I/O with the slot period operation engine 405 through the 2nd buffer memory 404. The 2nd buffer memory 404 stores a minute of data several times of one slot which is the batch of the slot period operation engine 405 as the input signal before processing is not overwritten. The 2nd buffer memory 404 is prepared for every channel.
[0033] The slot period operation engine 405 is a block which performs strange recovery processing in a slot unit. The slot period operation engine 405 performs I/O with the frame period operation engine 407 through the 3rd buffer memory 406. The 3rd buffer memory 406 is also prepared for every channel, and several time a minute of the data of one frame are stored, respectively.
[0034] The frame period operation engine 407 is a block which performs strange recovery processing in a frame unit. In addition, even when it is necessary to process in the unit of one or more frames by an interleave etc., it processes using a frame period operation engine similarly.
[0035] Each engine is controlled by the control engine 401. The channel which each engine 403,405,407 performs strange recovery processing to asynchronous, and is made into a processing object by control of the control engine 401 is also independent for every engine. strange recovery processing of a multiple channel with the processing effectiveness of the whole hardware high by this -- the time -- multiplex -- making -- having .
[0036] (1) The configuration of the receiving (recovery) section of the symbol period operation engine 403 is shown in symbol period operation engine 403 drawing 6 . A symbol period operation engine uses the arithmetic element of the Ex-OR computing element 503 and adder 504 grade as a processing element, and performs recovery processing by making one symbol into the minimum batch. The data for every chip are read from the first buffer memory 402 through the input interface 501. The Ex-OR computing element 503 performs an exclusive OR with the diffusion sign generated by the PN (diffusion sign) generator 502, and an adder 504 and a register 505 accumulate the result of an operation over one symbol. A accumulation result is written in the 2nd buffer memory 404 through the output

interface 506.
[0037] A sequencer 508 reads control instruction from program memory 509, and the instruction of operation to the receive section of a symbol period operation engine is given when a decoder 510 decodes the instruction. As a required instruction of operation, starting and stop instruction of the recovery processing to the input signal of one channel, assignment of the read-out and the write address to input/output interface 501,506, setting out of the internal-state value of the internal-state register 507 in the PN generator 502, and assignment of the reset timing of the register 505 for accumulation are included.
[0038] The symbol period operation engine shown in drawing 6 operates as a correlation computing element by considering the phase of the diffusion sign generated from the PN generator 502 as immobilization to the data inputted. It operates as slide correlator (matched filter) by on the other hand making the phase of the diffusion sign generated from the PN generator 502 slide. A change-over of such actuation is also performed by the instruction of operation from a sequencer 508. In addition, when operating as slide correlator, detection of peak timing is performed with the slot period engine of the next step.
[0039] The program (for example, content assignment of the diffusion ratio of a channel and the internal-state register of PN generator) over a multiple channel is stored in program memory 509. Therefore, the receive section of drawing 6 does not have the channel which can carry out recovery processing fixed. Moreover, since the read-out address to the input interface 501 can be specified by the program, the finger which carries out recovery processing is not fixed, either. therefore, the channel finger which the receive section of a symbol period engine operates a high speed rather than other operation engines, and carries out recovery processing further -- suitably -- specifying -- the time -- multiprocessing -- things -- the whole -- hardware effectiveness can be raised.
[0040] Furthermore, the receive section of a symbol period operation engine is a part with the most expensive operation load in order to process the signal of a chip rate or a sampling rate. Therefore, it is desirable when preparing more than one, and it being parallel, and making a receive section process raises the whole hardware effectiveness.
[0041] Moreover, the configuration which parallelizes a part of hardware of a receive section, and accelerates processing is shown in drawing 7 . For example, in the case of the CDMA communication system which performs a QPSK diffusion modulation, in order to perform phase correction, it is necessary to perform a correlation operation in each combination of the inphase (I) component (DATA_I) of a signal and a rectangular (Q) component (DATA_Q), and I component (PN_I) of a diffusion sign and Q component (PN_Q). Then, it is possible by preparing pair 906-1-4 of the Ex-OR computing element 903, an adder 904, and a register 905 for juxtaposition, and performing a correlation operation simultaneously to gather the effectiveness of processing with a latter slot period operation engine.
[0042] The configuration of the transmitting (modulation) section of the symbol period operation engine 403 is shown in drawing 8 . A symbol period operation engine uses the arithmetic element of the Ex-OR computing element 603 and adder 604 grade as a processing element, and performs modulation processing by making one symbol into the minimum batch. The data for every symbol are read from the 2nd buffer memory 404 through the input interface 601. The Ex-OR computing element 603 performs an exclusive OR with the diffusion sign generated by the PN generator 602, and gives a transmitted power value with an adder subtracter 604. The result of an operation is written in memory 606 through the memory interface 605.
[0043] In order to compound the sending signal of all send channels, the sending signal sent out to the same timing is accumulated. Therefore, through the memory interface 605, the sending signal sent out to the same timing is read from memory 606, and is added with the data (computing-element 603 output) and the adder subtracter 604 which were diffused. The added result is again written in memory 606 through the memory interface 605.
[0044] A sequencer 608 reads control instruction from program memory 609, and an instruction of operation in the transmitting section of a symbol period operation engine is given when a decoder 610

decodes the instruction. The channel which also processes the transmitting section by the program corresponding to a multiple channel is not fixed like a receive section.
[0045] In order that the transmitting section of a symbol period operation engine may also process the signal of a chip rate, it is the high part of an operation load. Therefore, it is desirable when preparing more than one, and it being parallel, and making the transmitting section process raises the whole hardware effectiveness.
[0046] (2) The configuration of the slot period operation engine 405 is shown in slot period operation engine 405 drawing 9 . A slot period operation engine is a block which processes the data of a symbol rate. Detection of peak timing, detection, and Rake composition are included in processing of slot period operation part as creation of a transmit format, and recovery processing as modulation processing.
[0047] As shown in drawing 1111 , processing with a slot period operation engine has two or more kinds of symbols, such as the receiving data symbol 1101, the pilot symbol 1102, the rate judging symbol 1103, and the power control symbol 1104, and needs to carry out different processing for every class of symbol.
[0048] However, all of these operations are the operations constituted as multiplication and addition and subtraction should combine. Then, the memory 702 and the register 703 in which a basic computing element (shift operation machine 706 for a multiplier 704, an adder subtracter 705, and digit doubling) and a count result are stored are connected by bus 708 and 709, and it considers as the configuration which added input/output interface 701,707 to this. The combination of the operation corresponding to each processing is beforehand described by program memory 711, a sequencer 710 gives the address of the program corresponding to each processing to program memory 711, and a decoder 512 decodes the read program. Input/output interface 701,707 and a bus 708,709 are controlled by the decoded control signal. The example of typical slot data processing is shown below.
[0049] (A) Processing to a pilot symbol (phase revolution detection)
With an adder subtracter 705, it is in phase, two or more pilot symbols are added, and the amplitude and topology on a propagation path are calculated.
[0050] First, a decoder 712 directs the address with which the pilot symbol went into the input interface 701, and directs to send data to a bus 708 from the input interface 701 at an adder subtracter 705. Thereby, a pilot symbol is sent to an adder subtracter 705 from the input interface 701. An adder subtracter 705 performs an add operation and, thereby, addition of a pilot symbol is performed.
[0051] Next, a decoder 712 directs to send data to a register 703 from an adder subtracter 705 into a bus 709. Thereby, an addition result is sent to a register 703.
[0052] Then, from program memory 711, the program which performs addition with the value and the pilot symbol from the input interface 701 which were stored in the register 703 is sent to a decoder 712.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the configuration of the baseband section of the first operation gestalt.
[Drawing 2] It is drawing showing the configuration of the baseband section of the second operation gestalt.
[Drawing 3] It is drawing showing the flow chart of the recovery processing in the second operation gestalt.
[Drawing 4] It is drawing showing the flow chart of the modulation processing in the second operation gestalt.
[Drawing 5] It is drawing showing the configuration of the baseband section of the third operation gestalt.
[Drawing 6] It is drawing showing the configuration of the receiving system of the symbol period operation engine of the third operation gestalt.
[Drawing 7] It is drawing showing the second example of a configuration of the receiving system of the symbol period operation engine of the third operation gestalt.
[Drawing 8] It is drawing showing the configuration of the transmitting system of the symbol period operation engine of the third operation gestalt.
[Drawing 9] It is drawing showing the configuration of the slot period operation engine of the third operation gestalt.
[Drawing 10] It is drawing showing the configuration of the frame period operation engine of the third operation gestalt.
[Drawing 11] It is drawing showing the relation between the frame in a W-CDMA system, and a slot format.
[Drawing 12] It is drawing showing the configuration of the conventional base station.
[Description of Notations]
100 ... An antenna, 101 ... The wireless section, 102-1 - s ... Strange recovery processing section, 107 ... The transmitting output composition section, 108-1 - n, 208-1 - n ... Correlation operation part, 111, 112, 113, 211-1 - n ... 114 The detection section, 214 ... Rake composition section, 115 215 ... 116 DEINTARIBA, 216 ... Error correction decoder, 117 217 ... 118 An error detection decoder, 218 ... Error detecting code machine, 119 219 ... 120 An error correcting code machine, 220 ... INTARIBA, 121 221 ... 122 A transmit format creation machine, 222 ... Diffusion operation part, 133 233 ... A transmitted power control section, 230 ... Strange recovery processing section, 235 ... A sector input selector, 236 ... Matched filter, 237 ... 134 A peak detecting element, 202 ... Baseband section, 201, 301, 402, 404, 406 ... Buffer memory, 302 ... CPU, 401 ... A control engine, 403 ... Symbol period operation engine, 405 ... A slot period operation engine, 407 ... Frame period operation engine, 501, 601, 701, 801 ... 502 An input interface, 602 ... PN generator, 503, 603, 903-1-4 ... An Ex-OR computing element, 504, 904-1-4 ... Adder, 505, 703, 803, 905-1-4 ... A register, 506, 707, 809 ... Output interface, 507 607 ... An internal-state register, 508, 608, 710, 812 ... Sequencer, 509, 609, 711, 813 ... Program

memory, 510, 610, 712, 814 ... Decoder, 604 705 ... An adder subtracter, 605 ... Memory interface, 606, 702, 802 ... Memory, 704 ... A multiplier, 706 ... Shift operation machine, 708 709 ... A bus, 804 ... An error detecting code-ized machine, 805 ... Error detection decoder, 806 ... An error correcting code-ized machine, 807 ... An error correction decoder, 808 ... Address computation computing element, 901, 902, 903, 904 ... The pair of an Ex-OR computing element and an adder, 1101 ... A data symbol, 1102 ... Pilot symbol, 1103 [... One symbol section, 1108 / ... One chip section.] ... A rate judging symbol, 1104 ... A power control symbol, the 1105...1-frame section, 1106 ... One slot section, 1107

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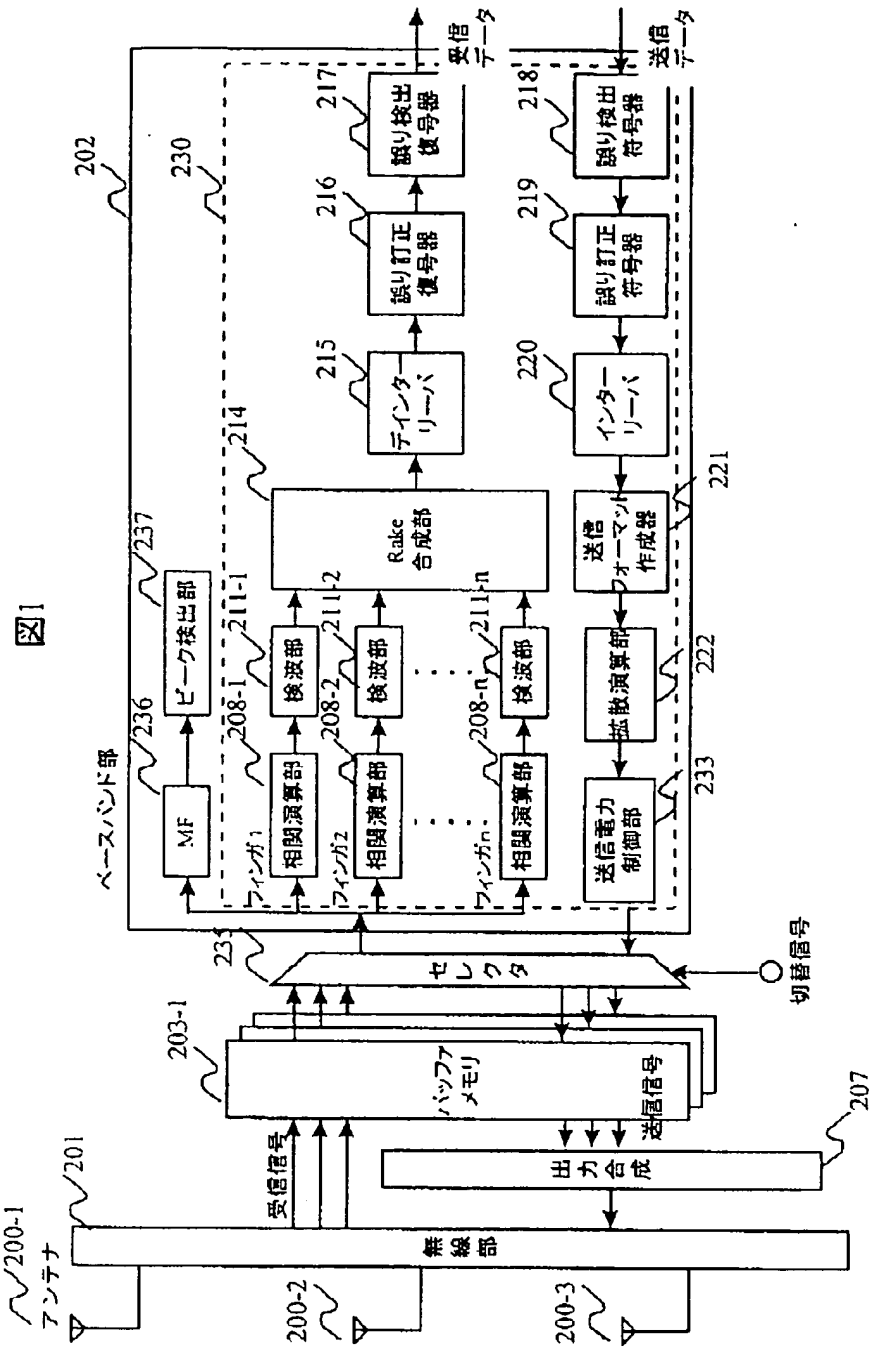
DRAWINGS

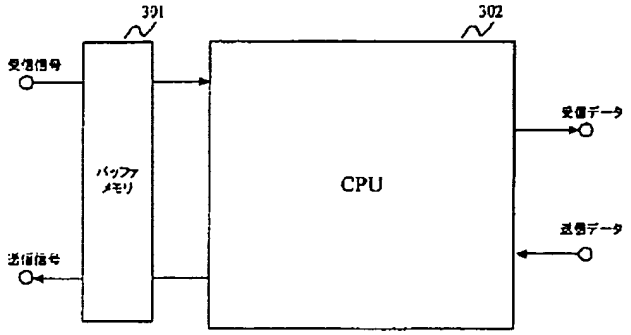
[Drawing 1]

図1


受信データ
送信データ
誤り検出復号器
誤り訂正復号器
デインターリーバ
Rake合成部
誤り検出符号器
誤り訂正符号器
インターリーバ
送信フォーマット作成器
ベースバンド部
MF
ピーク検出部
検波部
相関演算部
拡散演算部
送信電力制御部
セレクタ
切替信号
バッファメモリ
送信信号
受信信号
出力合成
無線部
アンテナ
フィンガ1
フィンガ2
フィンガn

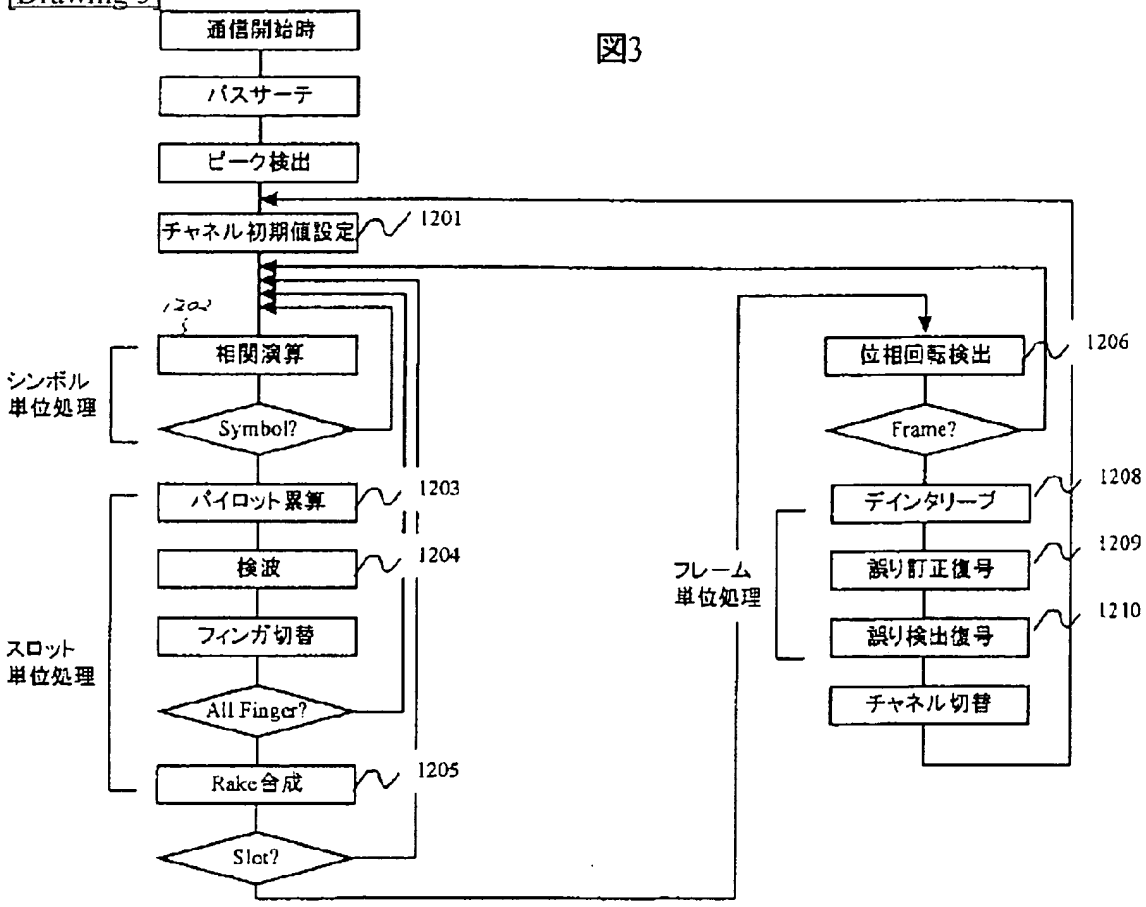
[Drawing 2]

図2



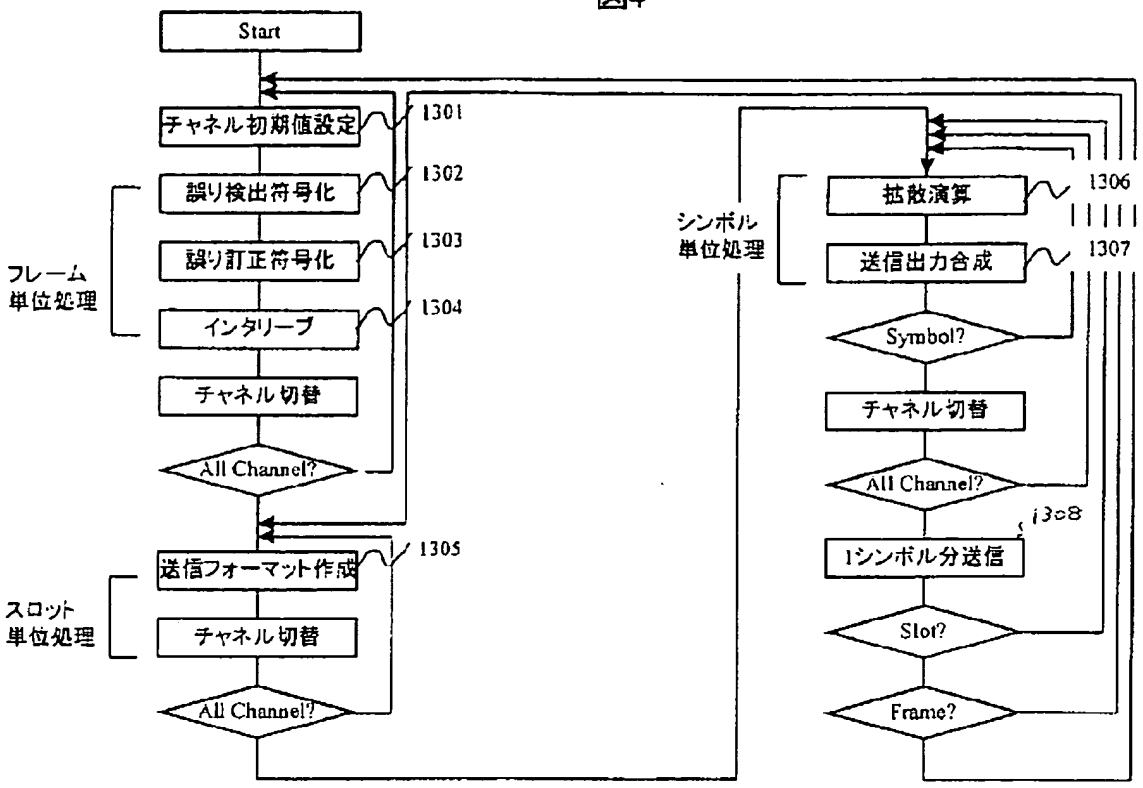
[Drawing 3]

図3



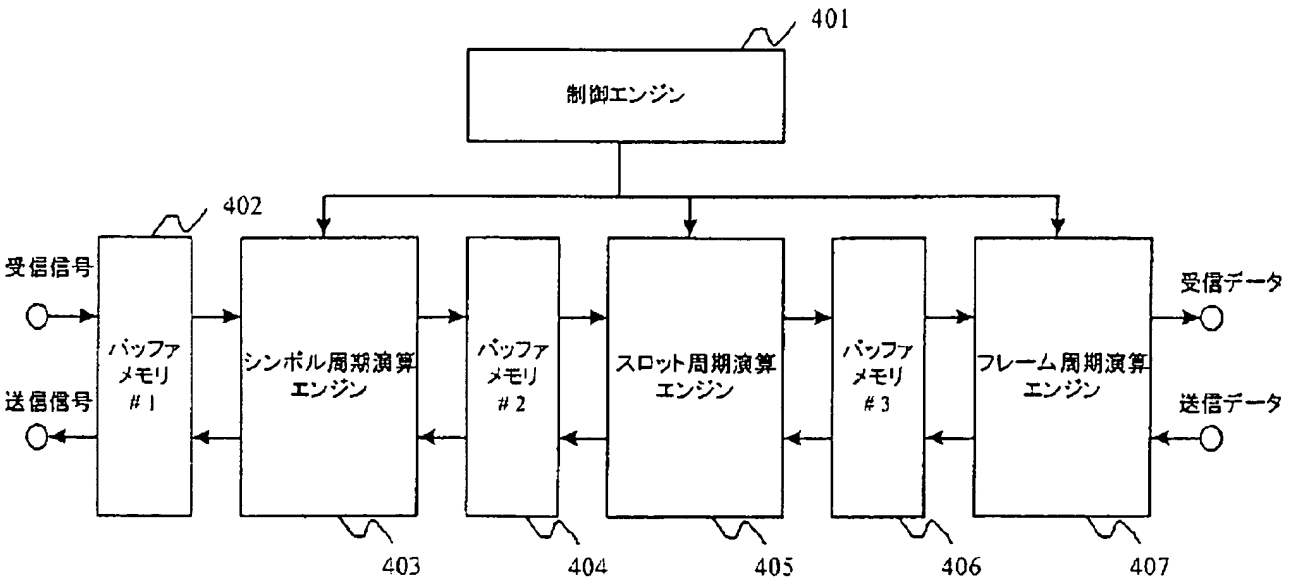
[Drawing 4]

図4



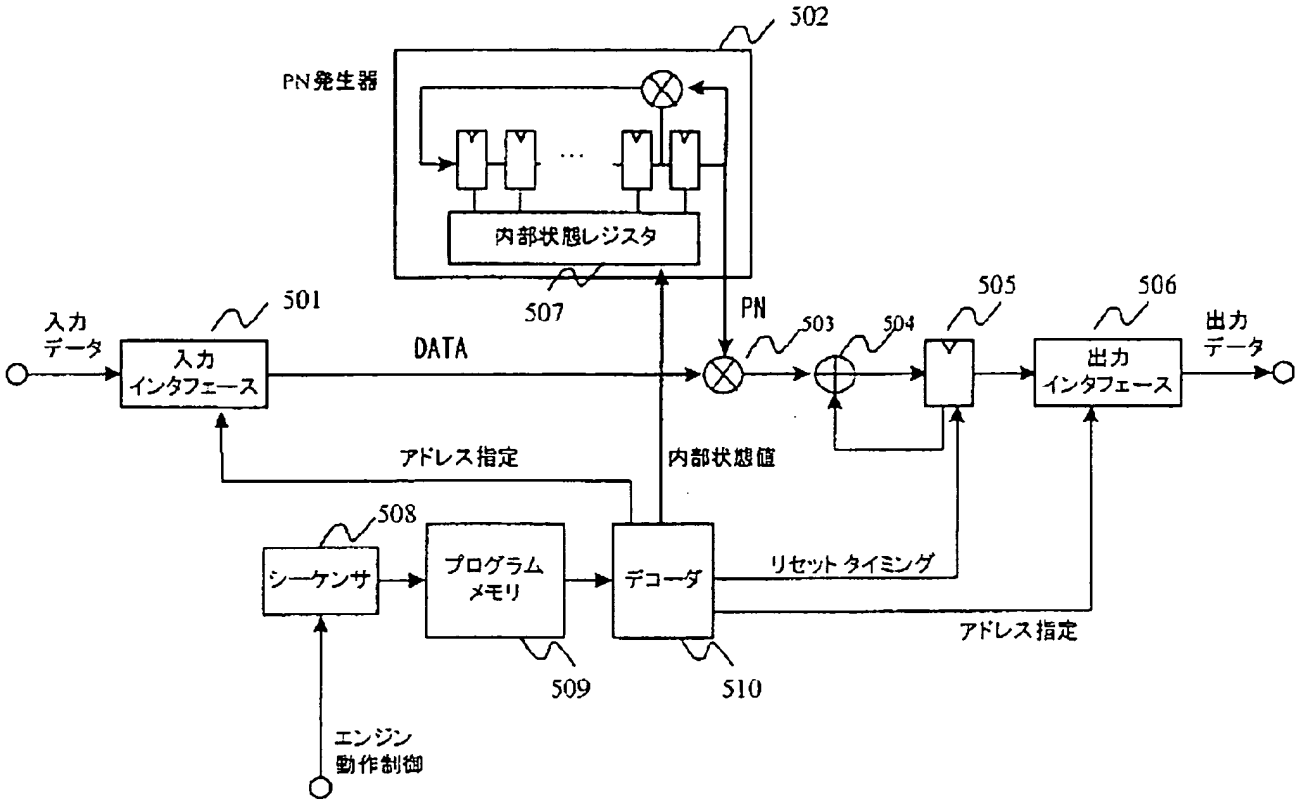
[Drawing 5]

図5



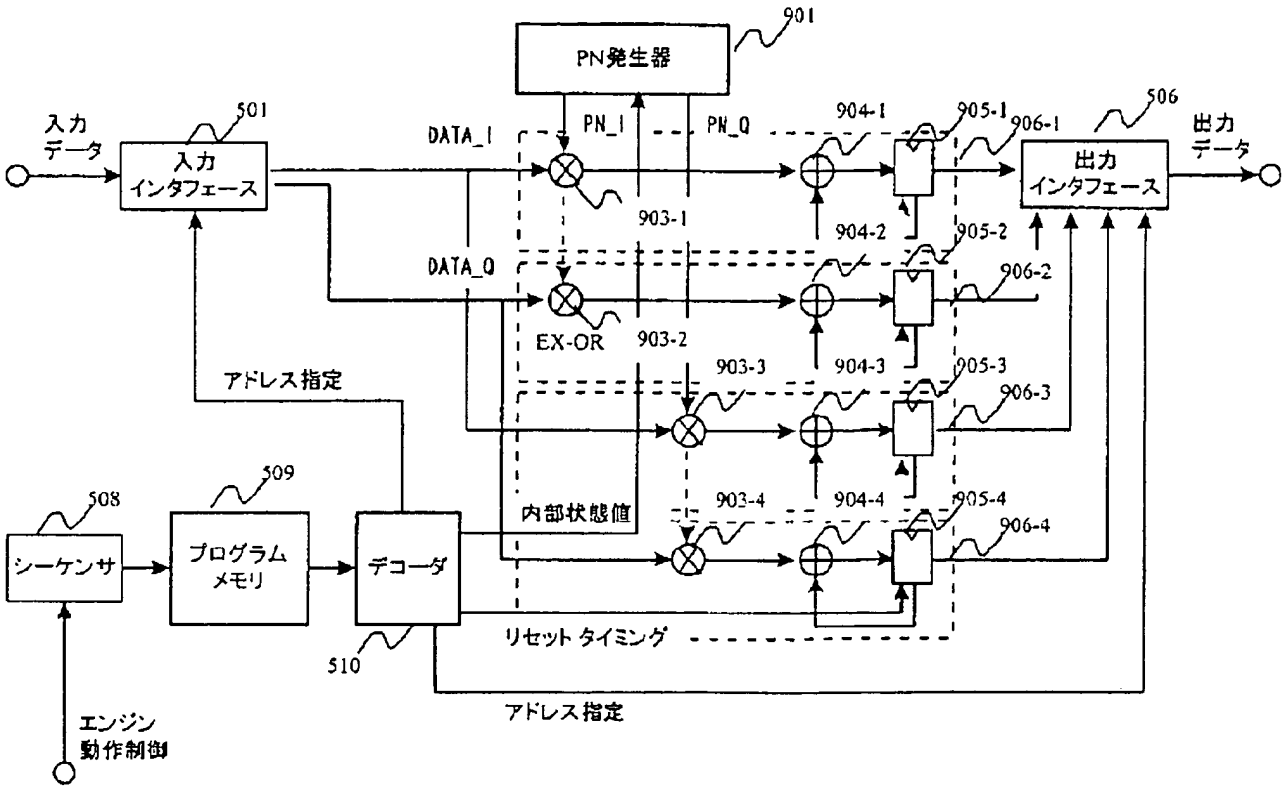
[Drawing 6]

図6



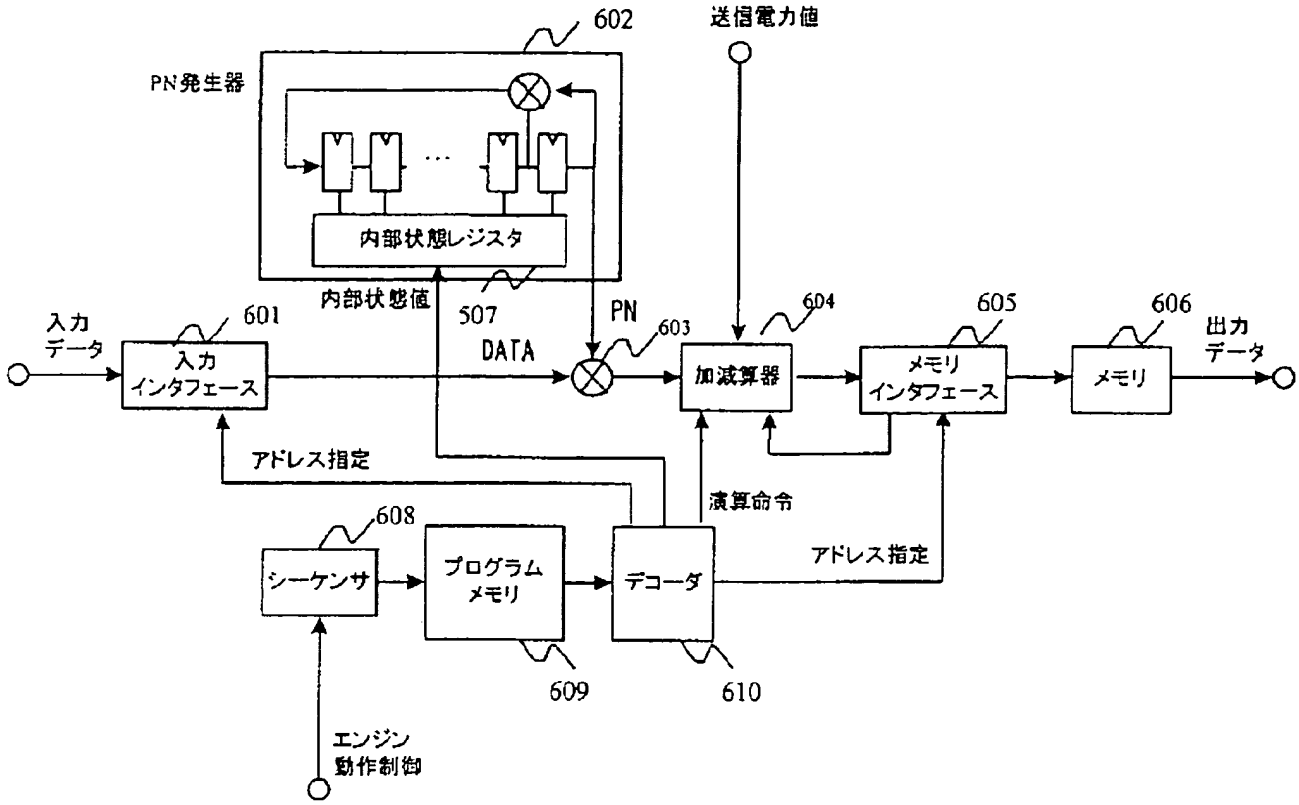
[Drawing 7]

図7



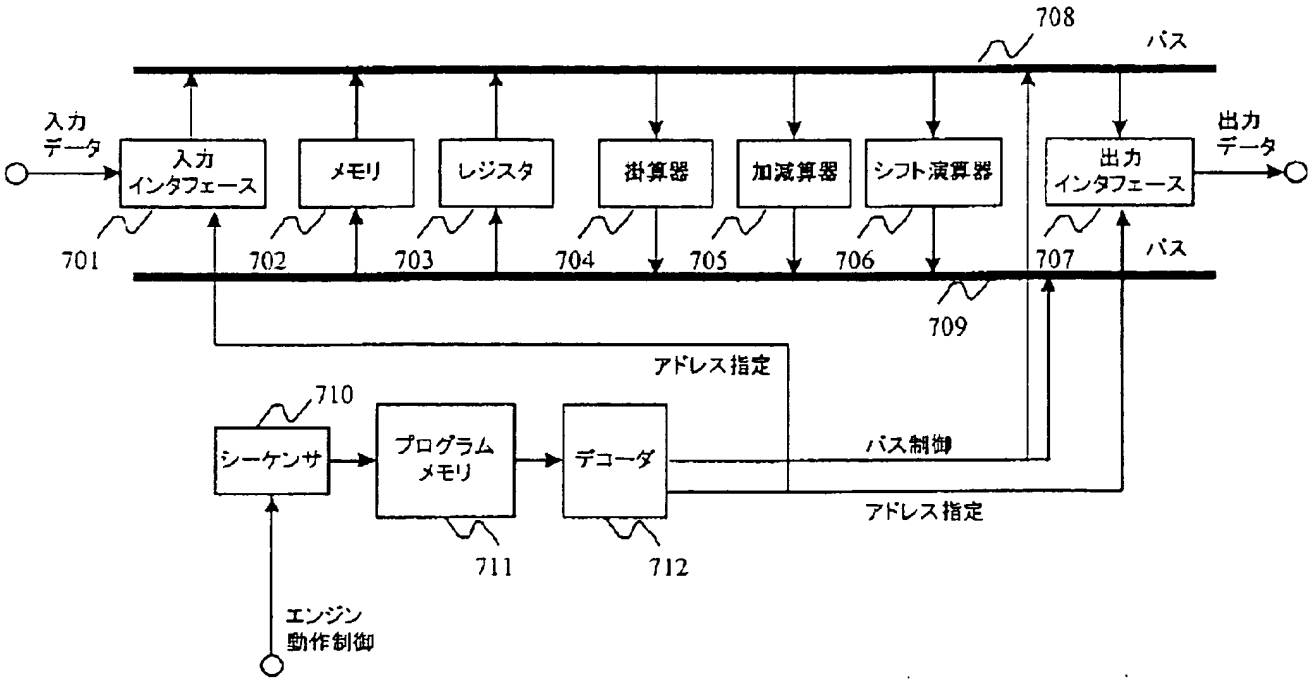
[Drawing 8]

図8



[Drawing 9]

図9



[Drawing 10]

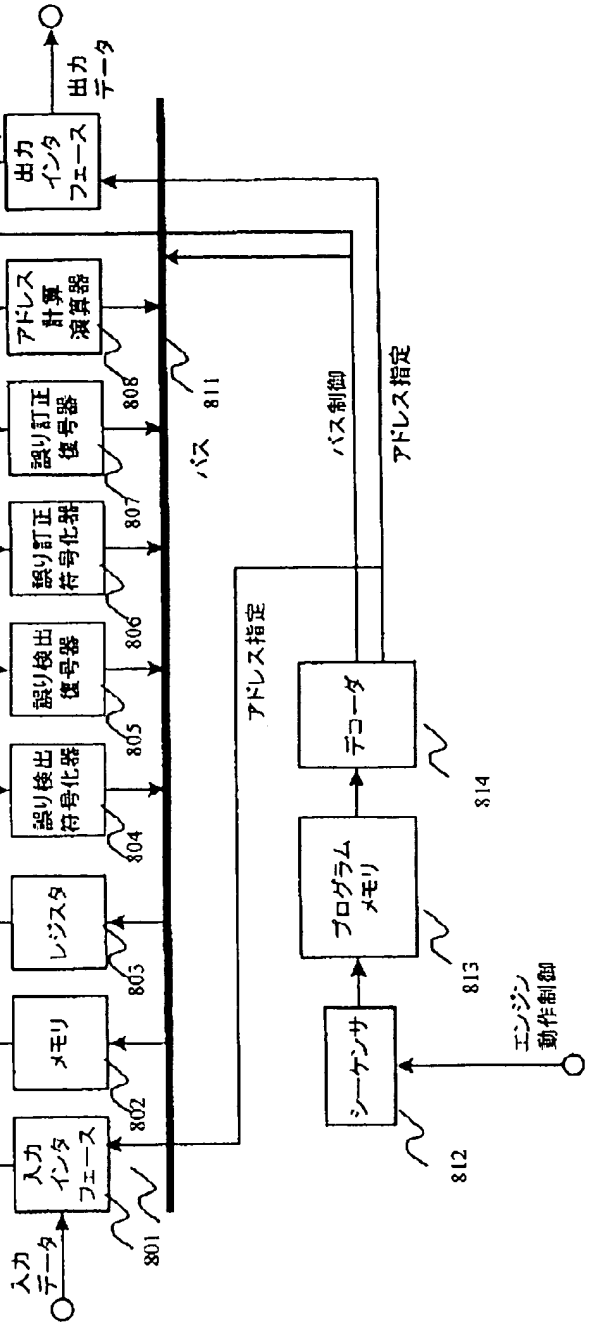
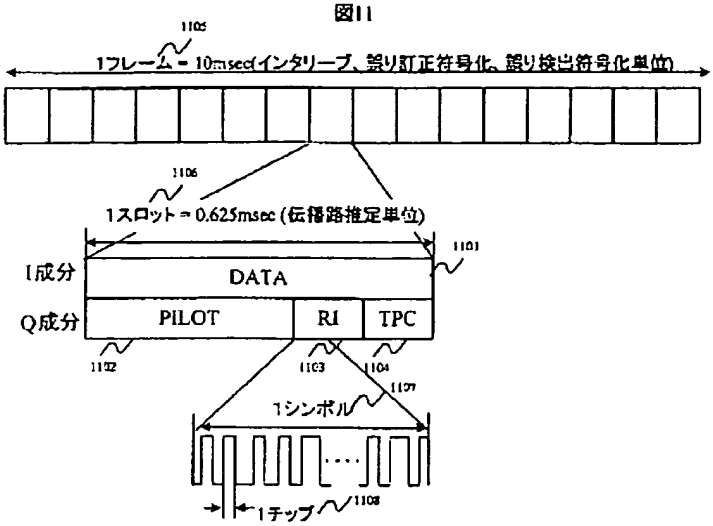


図10

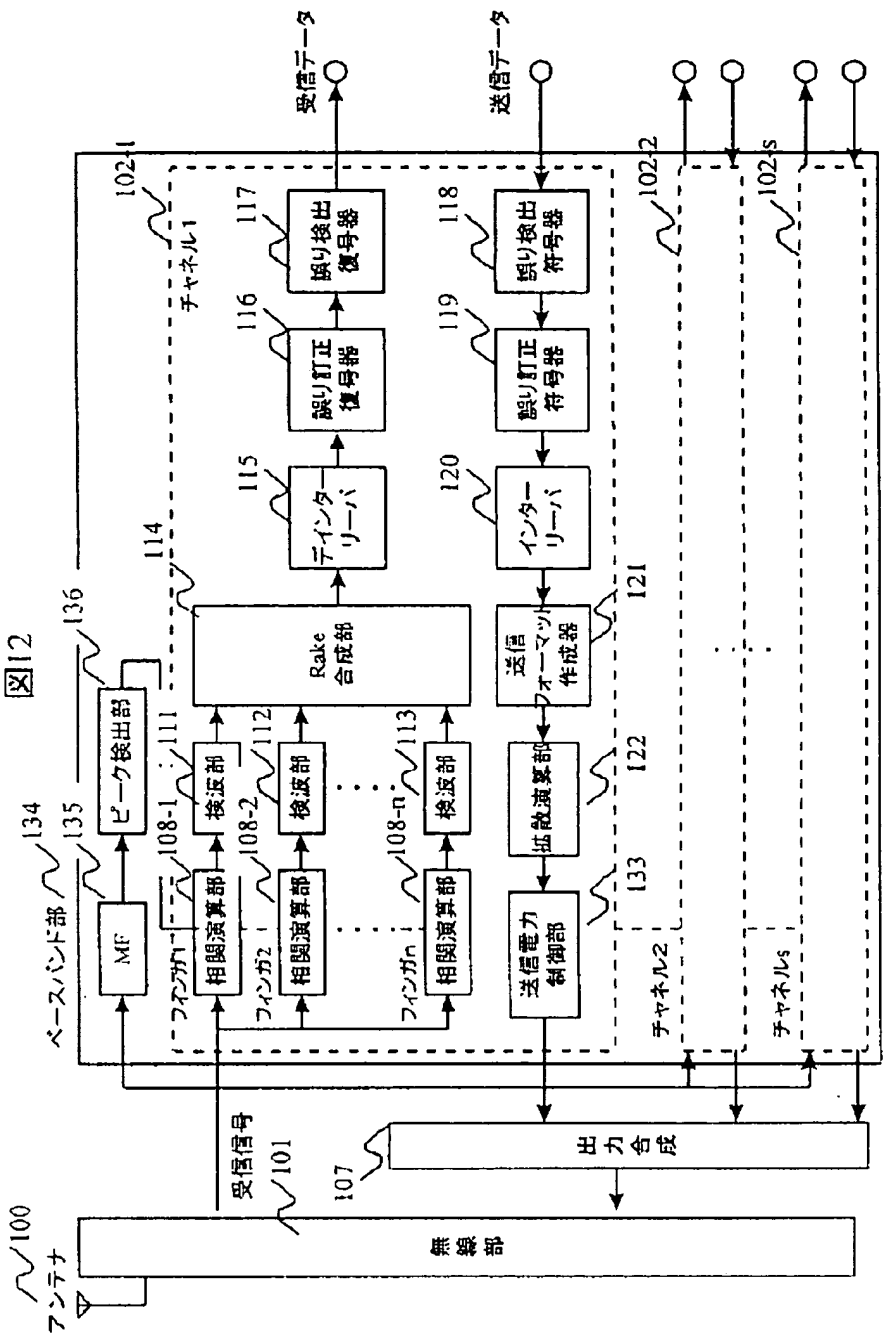
[Drawing 11]

図11



[Drawing 12]

図12



[Translation done.]